IS61WV25616LEBLL
IS64WV25616LEBLL

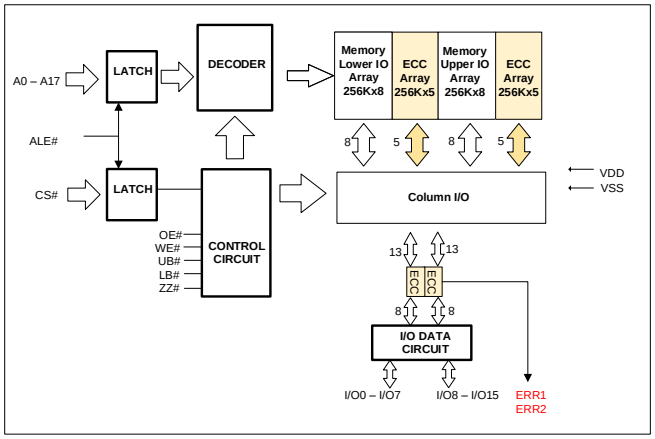
256Kx16 HIGH SPEED ASYNCHRONOUS CMOS STATIC RAM with LATCHED ADDRESS & ECC

PRELIMINARY INFORMATION
MARCH 2017

KEY FEATURES

- High-speed access time: 12ns, 15ns
- Single power supply
  - 2.4V-3.6V VDD
- Ultra Low Standby Current with ZZ# pin
  - IZZ = 30uA (typ.)
- Error Detection and Correction with optional ERR1/ERR2 output pin:
  - ERR1 pin indicates 1-bit error detection and correction.
  - ERR2 pin indicates multi-bit error detection
- ALE# pin to latch Address & CS# signals.
- Industrial and Automotive temperature support
- Lead-free available

FUNCTIONAL BLOCK DIAGRAM



The *ISSI* IS61/64WV25616LEBLL are high-speed, low power, 4M bit Latched static RAMs organized as 256K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology and implemented ECC function to improve reliability.

This highly reliable process coupled with innovative circuit design techniques including ECC (SEC-DED: Single Error Correcting-Double Error Detecting) yields high-performance and highly reliable devices.

When CS# is High (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels. Especially Ultra Low Standby Power at Snooze mode with ZZ# Low.

ALE# pin enables Address and CS# signals to be latched by asserting ALE# Low .

The IS61/64WV25616LEBLL are packaged in the JEDEC standard 48-pin mini BGA (6mm x 8mm), and 44-pin TSOP (TYPE II)

DESCRIPTION

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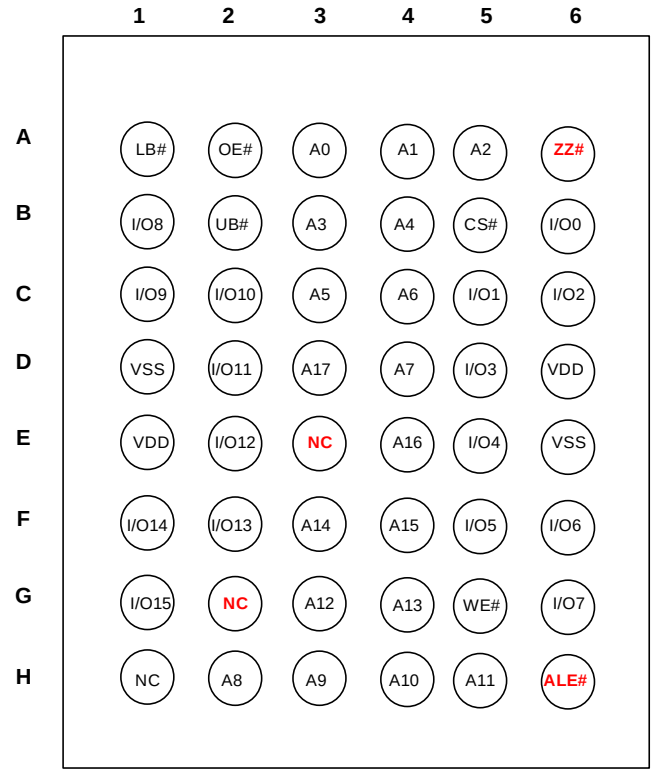
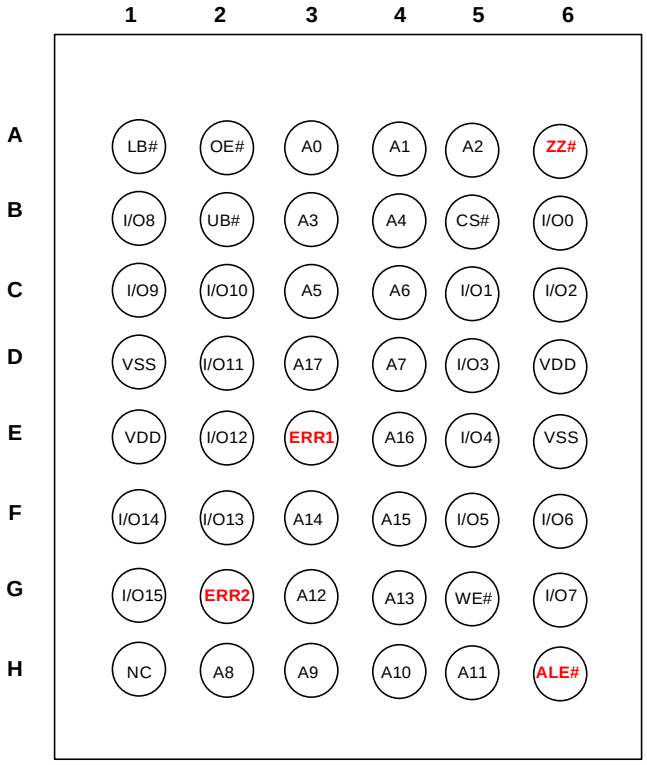
PIN CONFIGURATIONS

48-Pin mini BGA(6mm x 8mm) with ZZ#



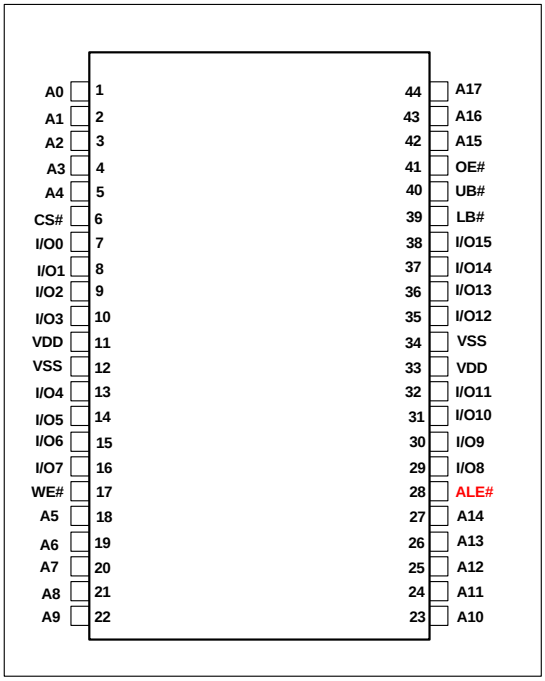
48-Pin mini BGA (6mm x 8mm) with ZZ# and ERR1/2



PIN DESCRIPTIONS

A0-A17	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CS#	Chip Enable Input
OE#	Output Enable Input
WE#	Write Enable Input
LB#	Lower-byte Control (I/O0-I/O7)
UB#	Upper-byte Control (I/O8-I/O15)
ERR1	1-bit Error Detection and Correction Signal
ERR2	2-bit ERR Detection Signal
ZZ#*	Power Sleep Mode. Ultra Low Standby current when Low.
ALE#	Address, CS# Latch Enable. Address, CS# latched on the falling edge of ALE#
NC	No Connection
VDD	Power
VSS	Ground

44-Pin TSOP-II



Notes:

1. ZZ# pin is internally pulled HIGH.

FUNCTION DESCRIPTION

Latched SRAM is the SRAM, which can latch Address/CS# inputs via ALE# pin. The address/CS# inputs will be latched when ALE# is Low, so the host could access another bus (Address/CS#) for the remaining operation period.

ADDRESS LATCH ENABLE (ALE#) FUNCTION

When Address Latch Enable signal (ALE#) is High, latch is transparent, and external address and CS# signals go through Address and CS# path to access memory cell array, and the device acts like normal Asynchronous SRAM.
When Address Latch Enable signal (ALE#) is Low, external address and CS# signals are latched, and those external signals are getting isolated from internal device (all other signals are not latched).
Memory controller does not have to maintain external address and CS# signals after ALE# goes Low during entire operation cycle, which could improve effective operation cycle time.
Also it could reduce potential glitch problem to achieve stable operation.

WRITE MODE

Write operation issues with Chip Select (CS#) Low and Write Enable (WE#) Low. The input and output pins (I/O0-15) are in data input mode. Output buffers are closed during this time even if OE# is Low. UB# and LB# enables a byte write feature. By enabling LB# Low, data from I/O pins (I/O0 through I/O7) are written into the location specified on the address pins. And with UB# being Low, data from I/O pins (I/O8 through I/O15) are written into the location.

READ MODE

Read operation issues with Chip Select (CS#) Low and Write Enable (WE#) High. When OE# is Low, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted. UB# and LB# enables a byte read feature. By enabling LB# Low, data from memory appears on I/O0-7. And with UB# being Low, data from memory appears on I/O8-15. OE# is Asynchronous pin to control output time.
In the READ mode, output buffers can be turned off by pulling OE# High. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

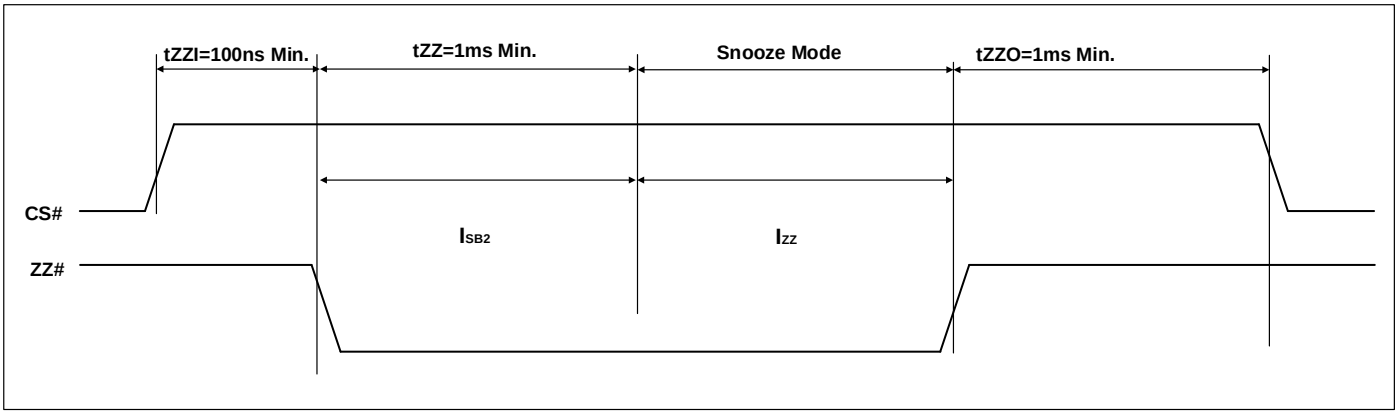
STANDBY MODE

Device enters standby mode when deselected (CS# HIGH). The input and output pins (I/O0-15) are placed in a high impedance state. The current consumption in this mode will be ISB1, or ISB2.

SNOOZE MODE

Device enters Snooze mode from Standby mode when asserting ZZ# Low, tZZI (100ns Min) after CS# High. Upon assertion of ZZ# Low, the device enters Snooze mode from Standby mode after tZZ (1ms Min.). During Snooze mode, the device must remain standby mode (CS# High), and ZZ# must remain asserted Low. Snooze mode can minimize Standby power consumption.
To exit Snooze mode, ZZ# must be de-asserted (High). The device returns to Standby mode from Snooze mode and CS# can be asserted Low, tZZO (1ms Min.) after de-assertion of ZZ# High.

SNOOZE MODE WAVEFORM



ERROR DETECTION AND ERROR CORRECTION

- Independent ECC per each byte
  - detect and correct 1-bit error per byte or detect multi-bit error per byte
- Optional ERR1 output signal indicates 1-bit error detection and correction
- Optional ERR2 output signal indicates multi-bit error detection.
- Controller can use either ERR1 or ERR2 to monitor ECC event. Unused pins (ERR1 or ERR2) can be left floating.
- Better reliability than parity code schemes which can only detect an error but not correct an error
- Backward Compatible: Drop in replacement to current in industry standard devices (without ECC)

ERR1, ERR2 OUTPUT SIGNAL BEHAVIOR

ERR1	ERR2	DQ pin	Status	Remark
0	0	Valid Q	No Error	
1	0	Valid Q	1-Bit Error only	1-bit error per byte detected and corrected
0	1	In-Valid Q	Multi-Bit Error only	No 1-bit error. Multi-bit error per byte detected (out of 2 bytes)
1	1	In-Valid Q	1-bit & Multi-bit error	1-bit error detected and corrected at one byte, and multi-bit error detected at another byte.
High-Z	High-Z	Valid D	Non-Read	Write operation or Output Disabled

TRUTH TABLE (ALE# IS HIGH)

Mode	CS#	ZZ# (1)	WE#	OE#	LB#	UB#	I/O0-I/O7	I/O8-I/O15	VDD Current
Not Selected	H	H	X	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	H	L	X	X	X	X	High-Z	High-Z	I_{ZZ}
Output Disabled	L	H	H	H	L	X	High-Z	High-Z	ICC,ICC1
	L	H	X	X	H	H	High-Z	High-Z	
Read	L	H	H	L	L	H	DOUT	High-Z	ICC,ICC1
	L	H	H	L	H	L	High-Z	DOUT	
	L	H	H	L	L	L	DOUT	DOUT	
Write	L	H	L	X	L	H	DIN	High-Z	ICC,ICC1
	L	H	L	X	H	L	High-Z	DIN	
	L	H	L	X	L	L	DIN	DIN	

Notes:

1. ZZ# pin can be left floating because it is internally pulled HIGH.

ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Vterm	Terminal Voltage with Respect to VSS	–0.5 to V_{DD} + 0.5V	V
V_{DD}	V_{DD} Related to VSS	–0.3 to 4.0	V
tStg	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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PIN CAPACITANCE (1)

Parameter	Symbol	Test Condition	Max	Units
Input capacitance	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DD}(typ)	6	pF
DQ capacitance (IO0–IO15)	$C_{I/O}$		8	pF

Note:
1. These parameters are guaranteed by design and tested by a sample basis only.

OPERATING RANGE(1)

Range	Ambient Temperature	PART NUMBER	SPEED (MAX)	VDD
Commercial	0°C to +70°C	IS61WV25616LEBLL	12 ns	2.4V – 3.6V
Industrial	-40°C to +85°C		12 ns	2.4V – 3.6V
Automotive (A1)	-40°C to +85°C	IS64WV25616LEBLL	12 ns	2.4V – 3.6V
Automotive (A3)	-40°C to +125°C	IS64WV25616LEBLL	12 ns	2.4V – 3.6V

Note:
1. Full device AC operation assumes a 100 µs ramp time from 0 to V_{DD}(min) and 200 µs wait time after V_{DD} stabilization.

THERMAL CHARACTERISTICS (1)

Parameter	Symbol	Rating	Units
Thermal resistance from junction to ambient (airflow = 1m/s)	$R_{\theta JA}$	TBD	°C/W
Thermal resistance from junction to pins	$R_{\theta JB}$	TBD	°C/W
Thermal resistance from junction to case	$R_{\theta JC}$	TBD	°C/W

Note:
1. These parameters are guaranteed by design and tested by a sample basis only.

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

Parameter	Unit (2.4V~3.6V)
Input Pulse Level	0.4V to V_{DD} -0.3V
Input Rise and Fall Time	1.0ns
Input and Output Timing and Reference Level (V_{REF})	V_{DD}/2
Output Load Conditions	Refer to Figure 1 and 2

OUTPUT LOAD CONDITIONS FIGURES

Figure1

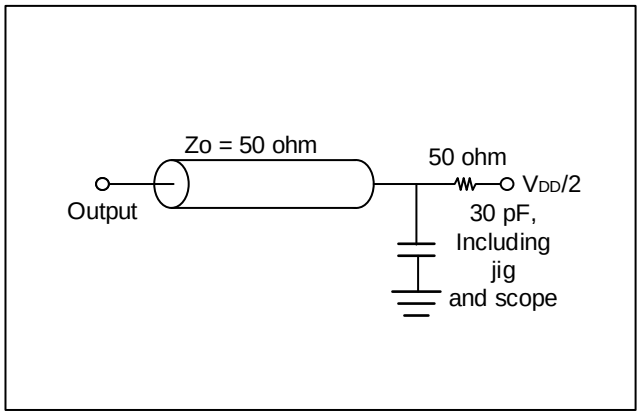
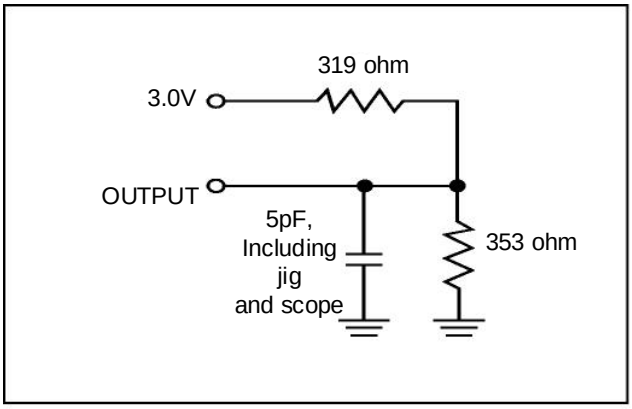


Figure2



DC ELECTRICAL CHARACTERISTICS

IS61(64)WV25616LEBLL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

VDD = 2.4V ~ 3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = -1.0 mA	1.8	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA	—	0.4	V
V_{IH}(1)	Input HIGH Voltage		2.0	V_{DD} + 0.3	V
V_{IL}(1)	Input LOW Voltage		–0.3	0.8	V
I_{LI}(2)	Input Leakage	VSS < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	VSS < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Notes:
1. VIL(min) = -0.3V DC ; VIL(min) = -2.0V AC (pulse width 2.0ns). Not 100% tested.
   VIH (max) = VDD + 0.3V DC ; VIH(max) = VDD + 2.0V AC (pulse width 2.0ns). Not 100% tested.
2. Input Leakage for ZZ# pin is +/-10uA because it is internally pulled HIGH.

POWER SUPPLY CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade	-12 Max.	-15 Max.	Unit
ICC	V_{DD} Dynamic Operating Supply Current	V_{DD} = MAX, I_{OUT} = 0 mA, f = f_{MAX}	Com.	60	55	mA
			Ind.	70	60	
			Auto.	80	75	
			Typ.(2)	40		
ICC1	Operating Supply Current	V_{DD} = MAX, I_{OUT} = 0 mA, f = 0	Com.	15	60	mA
			Ind.	20	80	
			Auto.	30	110	
ISB1	TTL Standby Current (TTL Inputs)	V_{DD} = MAX, V_{IN} = V_{IH} or V_{IL} CS# ≥ V_{IH}, f = 0	Com.	25	25	mA
			Ind.	30	30	
			Auto.	40	40	
ISB2	CMOS Standby Current (CMOS Inputs)	V_{DD} = MAX, CS# ≥ V_{DD} - 0.2V V_{IN} ≥ V_{DD} - 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	15	15	mA
			Ind.	20	20	
			Auto.	30	30	
			Typ.(2)	10		
IZZ	Snooze Mode Current (CMOS Inputs)	V_{DD} = MAX, CS# ≥ V_{DD} - 0.2V ZZ# ≤ 0.2V V_{IN} ≥ V_{DD} - 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	60	60	uA
			Ind.	80	80	
			Auto.	110	110	
			Typ.(2)	30		

Notes:
1. At f = fMAX, address and data inputs are cycling at the maximum frequency, f = 0 means no input line change.
2. Typical values are measured at V_{DD} = 3.0V, T_A = 25 °C and not 100% tested.

AC CHARACTERISTICS (OVER OPERATING RANGE)

READ CYCLE AC CHARACTERISTICS

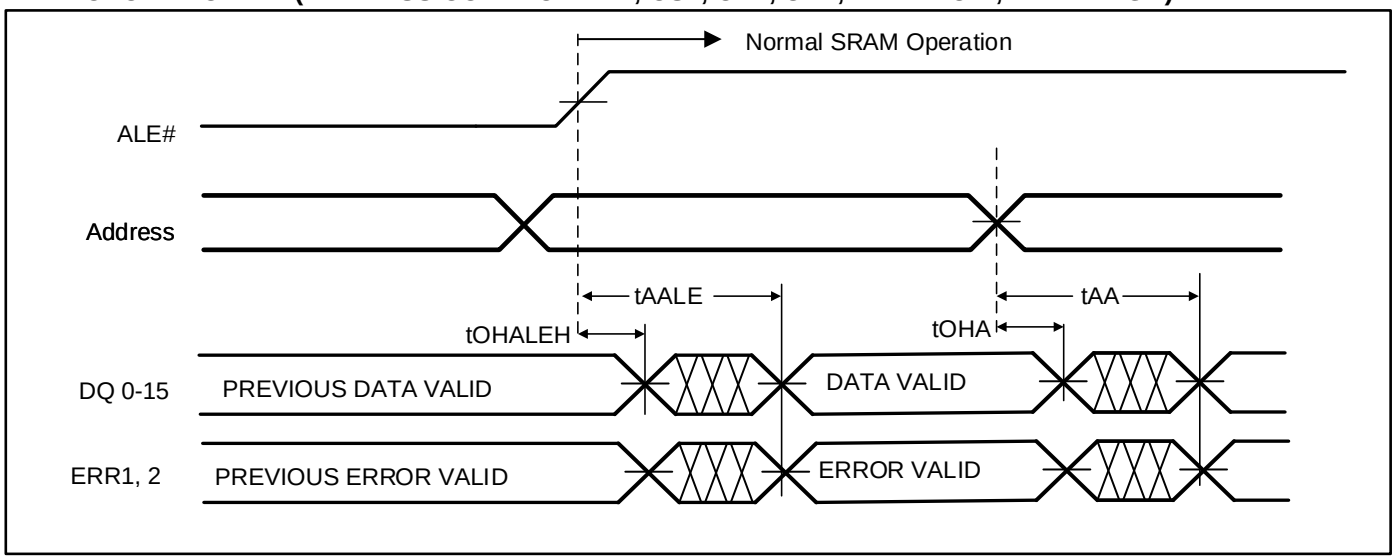
Parameter	Symbol	-12(1)		-15(1)		unit	notes
		Min	Max	Min	Max		
Read Cycle Time	tRC	12	-	15	-	ns	
Address Access Time	tAA	-	12	-	15	ns	
Output Hold Time	tOHA	3	-	3	-	ns	4
CS# Access Time	tACS	-	12	-	15	ns	
OE# Access Time	tDOE	-	6	-	8	ns	
OE# to High-Z Output	tHZOE	-	6	-	8	ns	2
OE# to Low-Z Output	tLZOE	0	-	0	-	ns	2
CS# to High-Z Output	tHZCS	-	6	-	8	ns	2
CS# to Low-Z Output	tLZCS	3	-	4	-	ns	2
UB#, LB# Access Time	tBA	-	6	-	8	ns	
UB#, LB# to High-Z Output	tHZB	-	6	-	8	ns	2
UB#, LB# to Low-Z Output	tLZB	0	-	0	-	ns	2
ALE# HIGH Access Time	tAALE	12	-	15	-	ns	
ALE# HIGH to Output Hold Time	tOHALEH	3	-	4	-	ns	3
Address Setup to ALE# LOW	tASALEL	3	-	4	-	ns	
CS# Setup to ALE# LOW	tCSALEL	3	-	4	-	ns	
Address Hold from ALE# LOW	tAHALEL	2	-	2.5	-	ns	
CS# Hold from ALE# LOW	tCHALEL	2	-	2.5	-	ns	
ALE# High Pulse Width	tALEP	3	-	4	-	ns	

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of VDD/2, and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. tOHALEH is output hold time when ALE# is transitioning to High, and tOHA is output hold time when ALE# stays High and Address is transitioning.

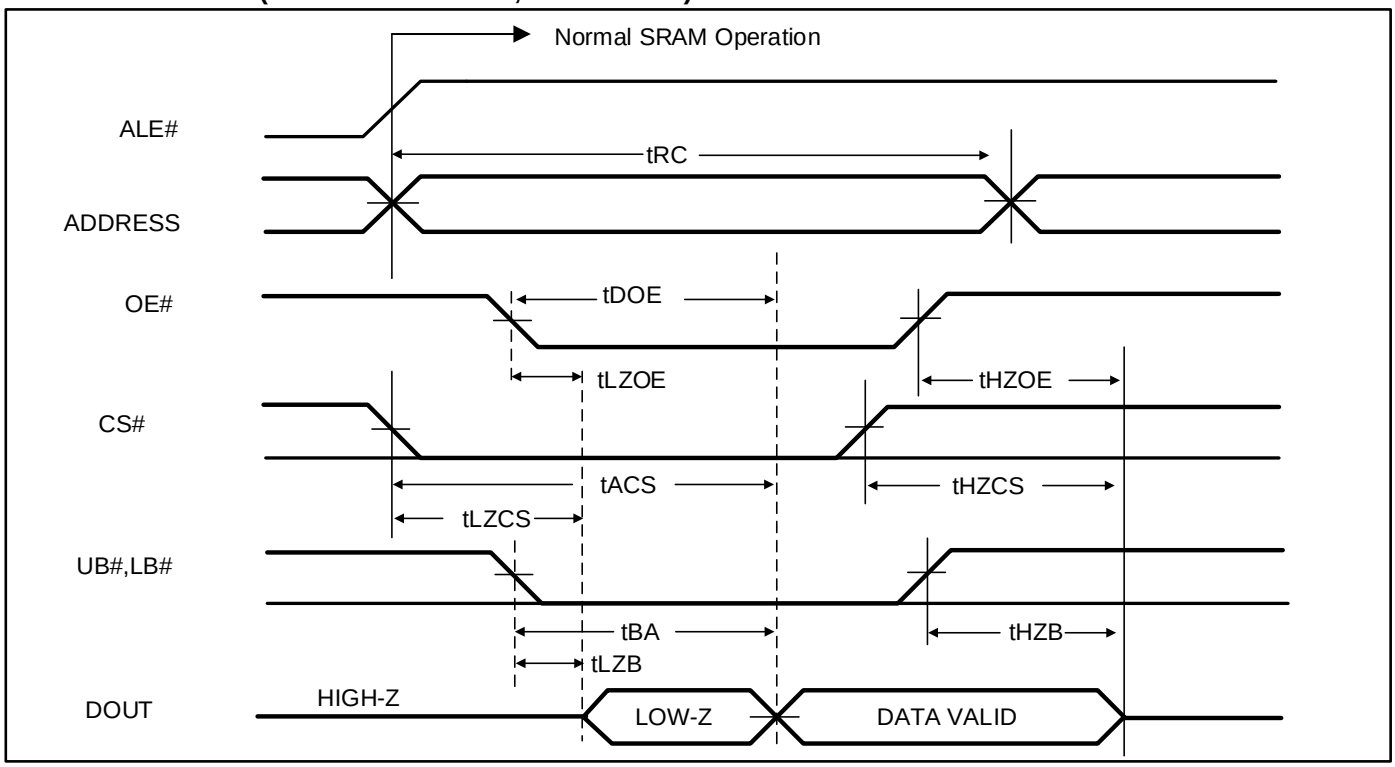
Timing Diagram

READ CYCLE NO. 1[1,2] (ADDRESS CONTROLLED , CS#, OE#, UB#, LB# = LOW, WE# = HIGH)

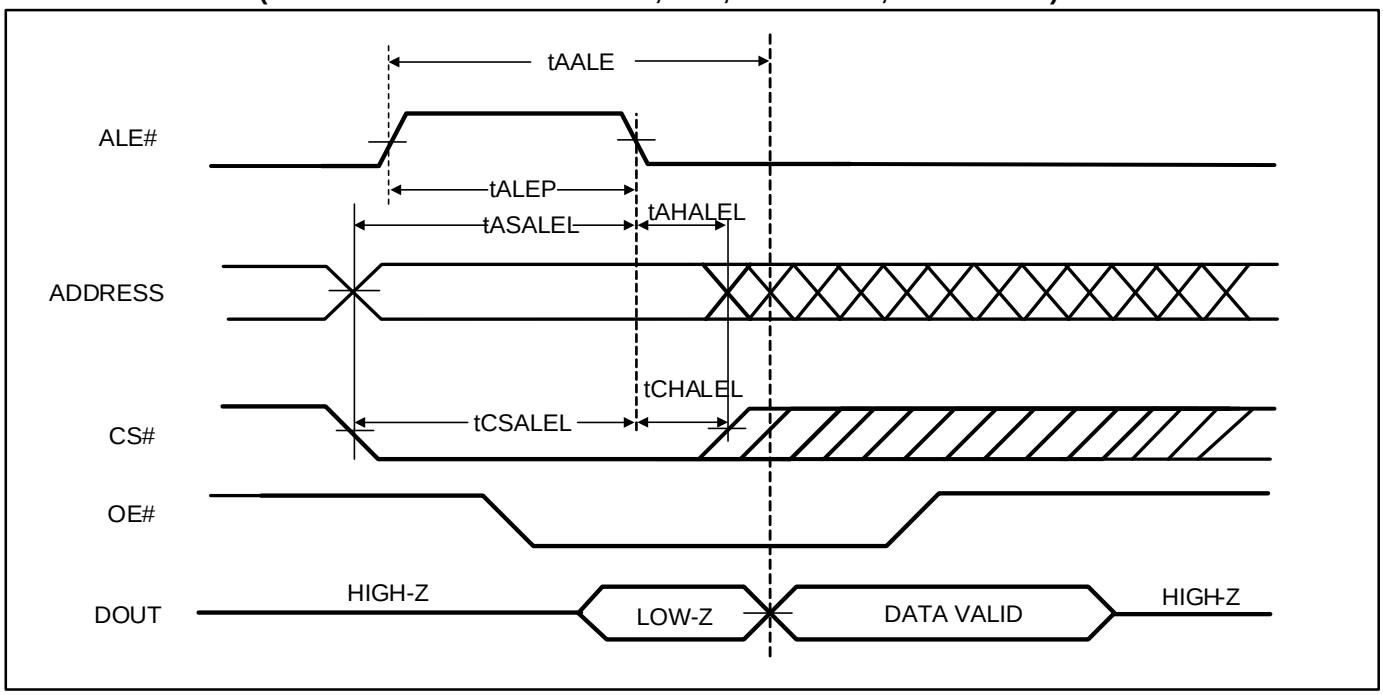


Notes:
1. Normal SRAM Operation when ALE# = HIGH
2. ERR1, ERR2 signals act like a Read Data Q during Read Operation.

READ CYCLE NO. 2 (OE# CONTROLLED, WE# = HIGH)



READ CYCLE NO. 3 (ALE# AND OE# CONTROLLED, UB#, LB# = LOW, WE# = HIGH)



WRITE CYCLE AC CHARACTERISTICS

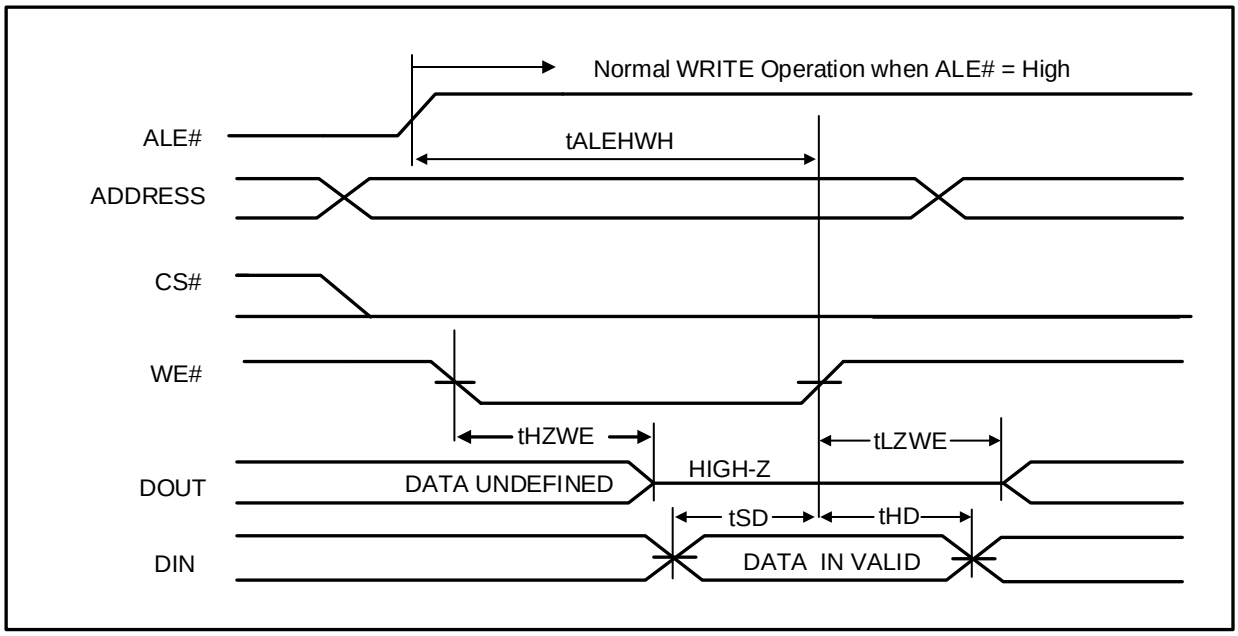
Parameter	Symbol	-12(1)		-15(1)		unit	notes
		Min	Max	Min	Max		
Write Cycle Time	tWC	12	-	15	-	ns	
CS# to Write End	tSCS	8	-	10	-	ns	
Address Setup Time to Write End	tAW	8	-	10	-	ns	
UB#,LB# to Write End	tPWB	8	-	10	-	ns	
Address Hold from Write End	tHA	0	-	0	-	ns	
Address Setup Time	tSA	0	-	0	-	ns	
WE# Pulse Width	tPWE1	8	-	10	-	ns	
WE# Pulse Width (OE#=LOW)	tPWE2	12	-	15	-	ns	4
Data Setup to Write End	tSD	6	-	8	-	ns	
Data Hold from Write End	tHD	0	-	0	-	ns	
WE# LOW to High-Z Output	tHZWE	-	6	-	8	ns	2
WE# HIGH to Low-Z Output	tLZWE	3	-	4	-	ns	2
ALE# HIGH to Write End	tALEHWH	8	-	10	-	ns	
Address Setup to ALE# LOW	tASALEL	3	-	4	-	ns	
CS# Setup to ALE# LOW	tCSALEL	3	-	4	-	ns	
Address Hold from ALE# LOW	tAHALEL	2	-	2.5	-	ns	
CS# Hold from ALE# LOW	tCHALEL	2	-	2.5	-	ns	
ALE# High Pulse Width	tALEP	3	-	4	-	ns	

Notes:

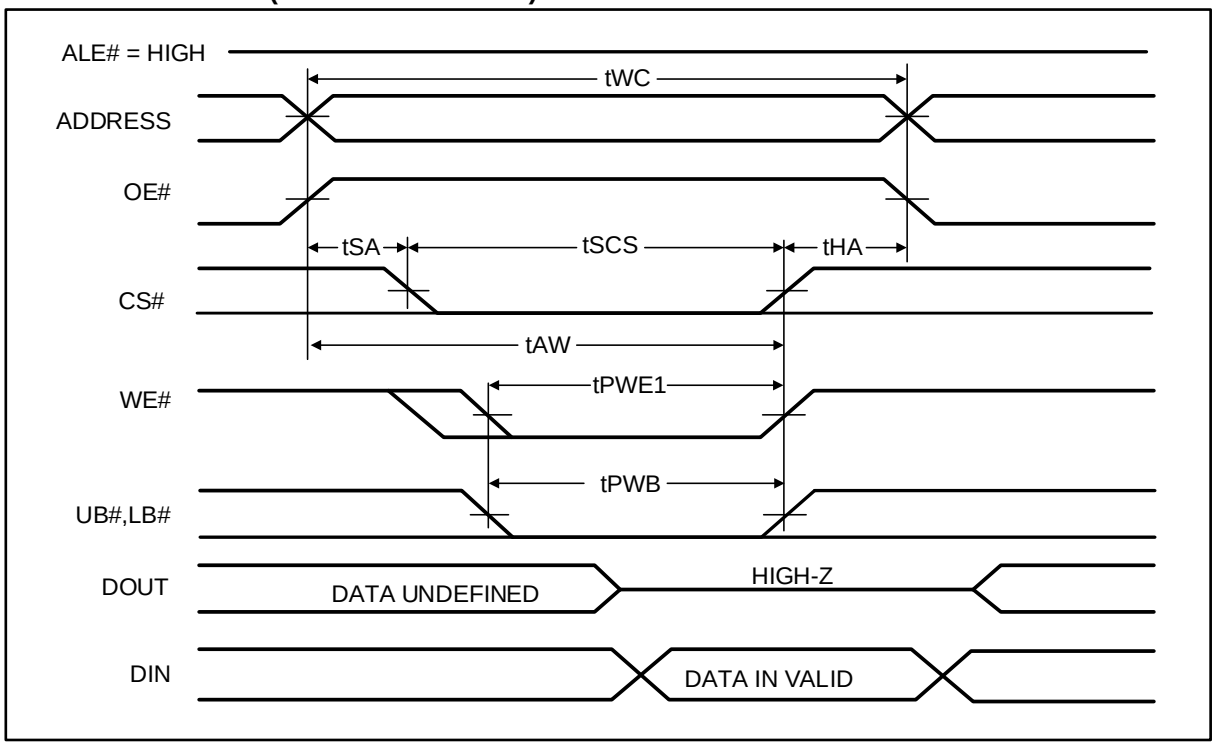
1 Test conditions assume signal transition times of 3 ns or less, timing reference levels of VDD/2, and output loading specified in Figure 1.
2 Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3 The internal write time is defined by the overlap of CS# =LOW, UB# or LB# =LOW, and WE# =LOW. All signals must be in valid states to initiate a Write, but anyone can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4 If OE# is low during write cycle, (WE# controlled, CS# = UB# =LB#= LOW, ALE#=HIGH), the minimum Write cycle time for write cycle NO.3 is the sum of tHZWE and tSD.

Timing Diagram

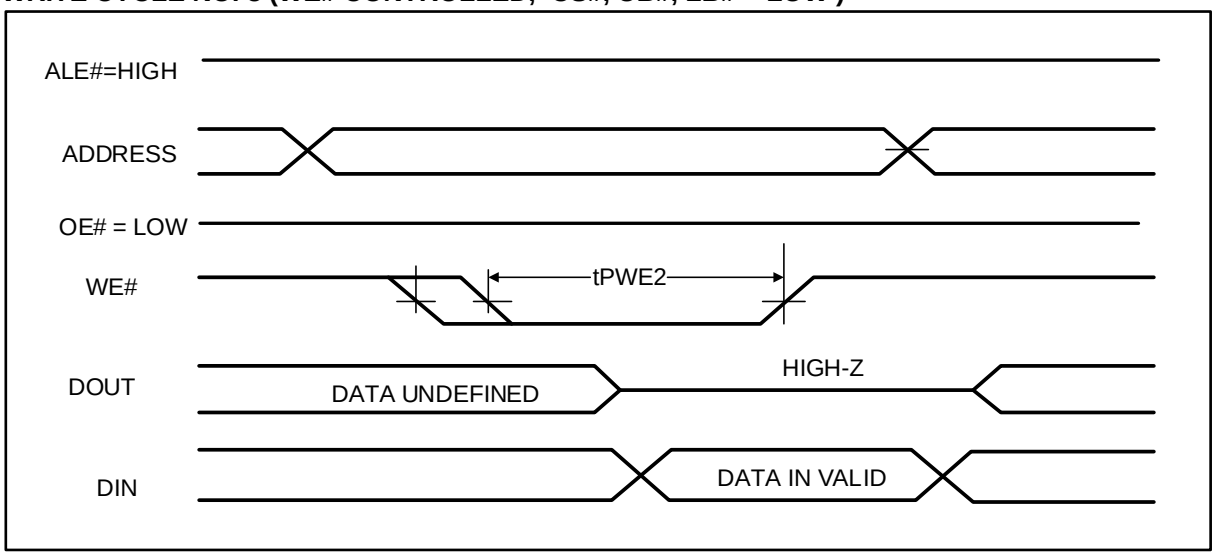
WRITE CYCLE NO. 1 (WE# CONTROLLED, UB#, LB# = LOW, OE# = HIGH)



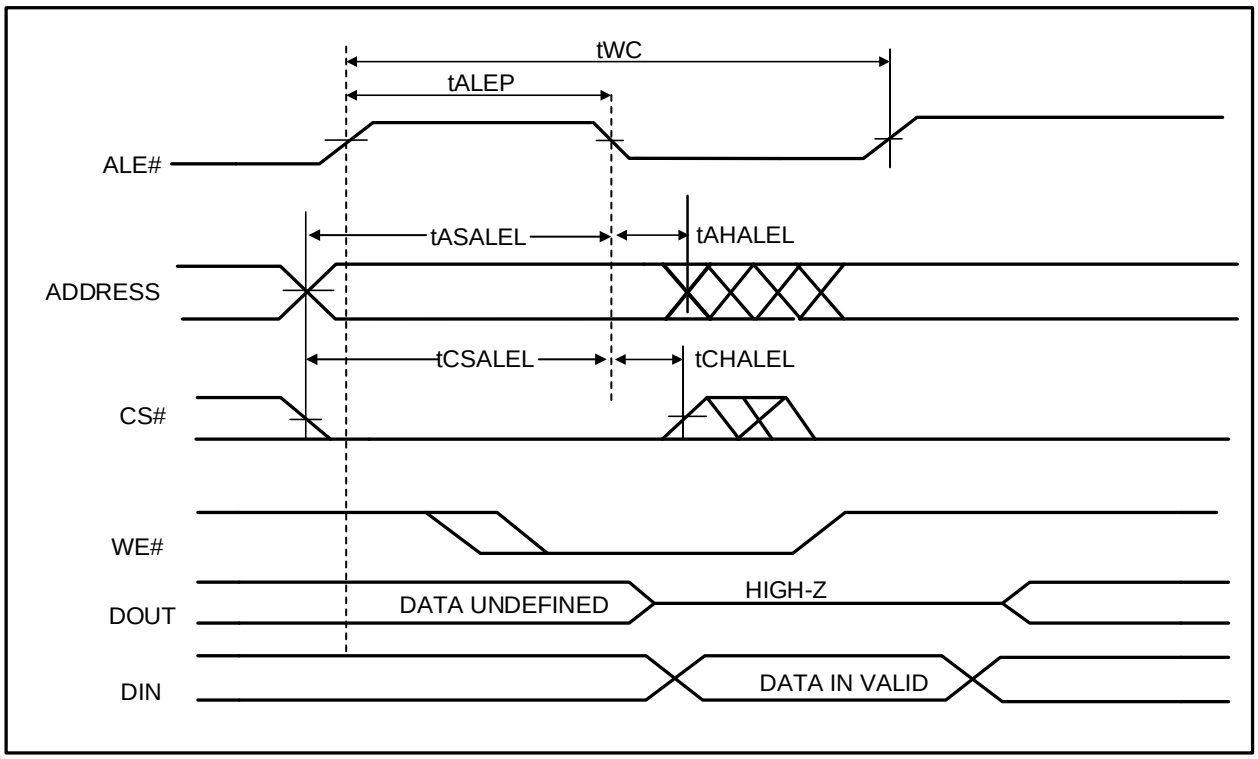
WRITE CYCLE NO. 2 (WE# CONTROLLED)



WRITE CYCLE NO. 3 (WE# CONTROLLED, CS#, UB#, LB# = LOW)



WRITE CYCLE NO. 4 (ALE# and WE# CONTROLLED, OE# = HIGH, UB#, LB# = LOW)

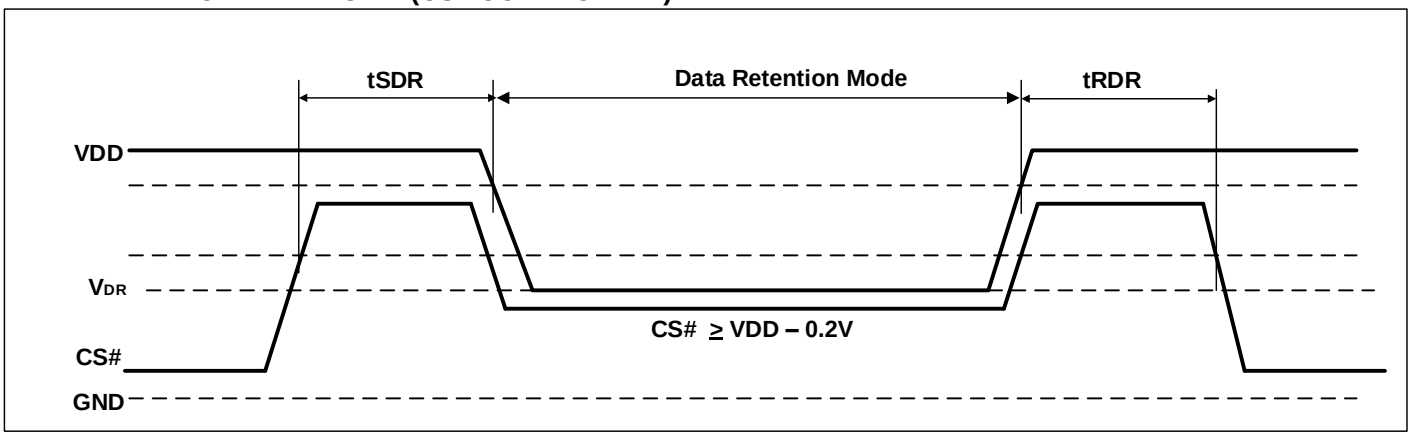


DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition	OPTION	Min.	Typ.(2)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0		3.6	V
I_{DR}	Data Retention Current	V_{DD}= MAX, CS# ≥ V_{DD} – 0.2V	Com.	-	10	15	mA
			Ind.	-	-	20	
			Auto	-	-	30	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	-	-	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		tRC	-	-	ns

Notes:
1. If CS# >VDD–0.2V, all other inputs including UB# and LB# must meet this condition.
2. Typical values are measured at VDD=3.0V, TA = 25℃ and not 100% tested.

DATA RETENTION WAVEFORM (CS# CONTROLLED)



ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
12	IS61WV25616LEBLL-12BI	mini BGA (6mm x 8mm)
12	IS61WV25616LEBLL-12BLI	mini BGA (6mm x 8mm), Lead-free
12	IS61WV25616LEBLL-12B2I	mini BGA (6mm x 8mm), ERR1/ERR2 Pins
12	IS61WV25616LEBLL-12B2LI	mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
12	IS61WV25616LEBLL-12TI	TSOP (Type II)
12	IS61WV25616LEBLL-12TLI	TSOP (Type II), Lead-free
15	IS61WV25616LEBLL-15BI	mini BGA (6mm x 8mm)
15	IS61WV25616LEBLL-15BLI	mini BGA (6mm x 8mm), Lead-free
15	IS61WV25616LEBLL-15B2I	mini BGA (6mm x 8mm), ERR1/ERR2 Pins
15	IS61WV25616LEBLL-15B2LI	mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
15	IS61WV25616LEBLL-15TI	TSOP (Type II)
15	IS61WV25616LEBLL-15TLI	TSOP (Type II), Lead-free

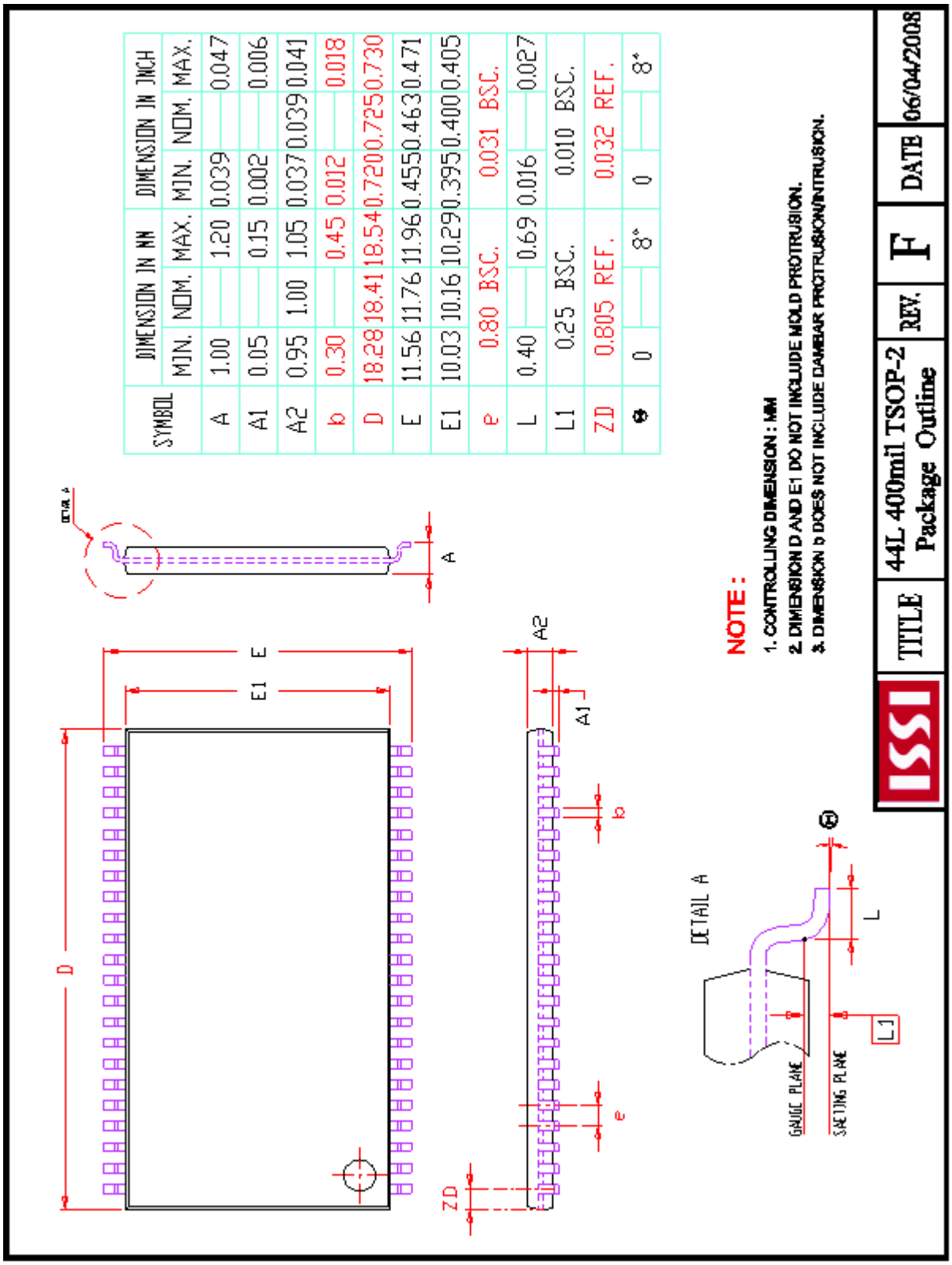
AUTOMOTIVE RANGE (A1): –40°C TO +85°C

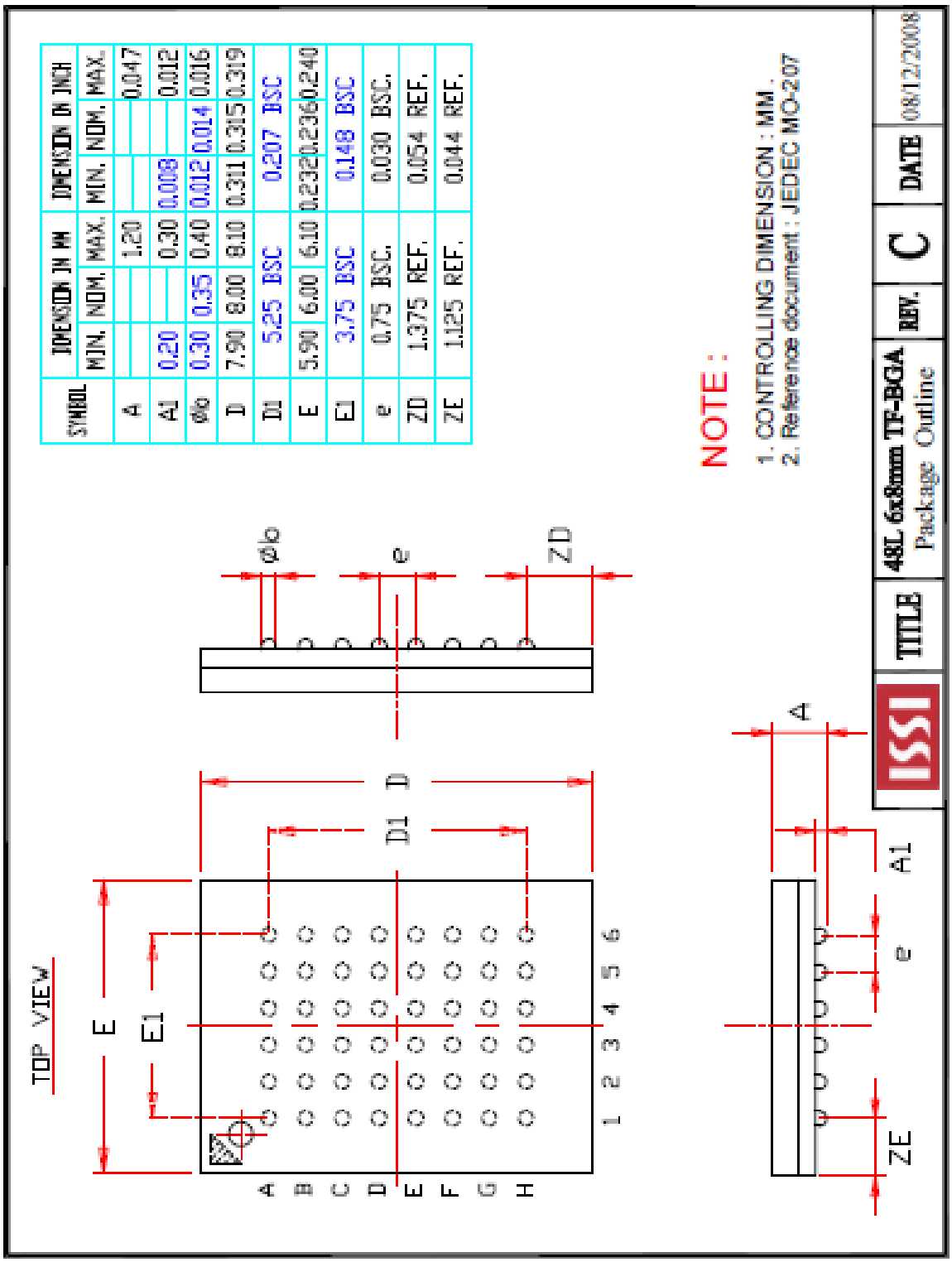
Speed (ns)	Order Part No.	Package
12	IS64WV25616LEBLL-12BA1	mini BGA (6mm x 8mm)
12	IS64WV25616LEBLL-12BLA1	mini BGA (6mm x 8mm), Lead-free
12	IS64WV25616LEBLL-12B2A1	mini BGA (6mm x 8mm), ERR1/ERR2 Pins
12	IS64WV25616LEBLL-12B2LA1	mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
12	IS64WV25616LEBLL-12CTA1	TSOP (Type II), Copper Leadframe
12	IS64WV25616LEBLL-12CTLA1	TSOP (Type II), Copper Leadframe , Lead-free

AUTOMOTIVE RANGE (A3): –40°C TO +125°C

Speed (ns)	Order Part No.	Package
12	IS64WV25616LEBLL-12BA3	mini BGA (6mm x 8mm)
12	IS64WV25616LEBLL-12BLA3	mini BGA (6mm x 8mm), Lead-free
12	IS64WV25616LEBLL-12B2A3	mini BGA (6mm x 8mm), ERR1/ERR2 Pins
12	IS64WV25616LEBLL-12B2LA3	mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
12	IS64WV25616LEBLL-12CTA3	TSOP (Type II), Copper Leadframe
12	IS64WV25616LEBLL-12CTLA3	TSOP (Type II), Copper Leadframe, Lead-free

PACKAGE INFORMATION




SYMBOL
DIMENSION IN MM
MIN. NOM. MAX.
DIMENSION IN INCH
MIN. NOM. MAX.
A — — 1.20 — — 0.047
A1 0.20 — 0.30 0.008 — 0.012
ϕb 0.30 0.35 0.40 0.012 0.014 0.016
D 7.90 8.00 8.10 0.311 0.315 0.319
D1 5.25 BSC 0.207 BSC
E 5.90 6.00 6.10 0.232 0.236 0.240
E1 3.75 BSC 0.148 BSC
e 0.75 BSC. 0.030 BSC.
ZD 1.375 REF. 0.054 REF.
ZE 1.125 REF. 0.044 REF.
NOTE :
1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207
TOP VIEW
ϕb
e
ZD
D
D1
E
E1
A
A1
ZE
1 2 3 4 5 6
A B C D E F G H
TITLE
48L 6x8mm TF-BGA
Package Outline
REV.
C
DATE
08/12/2008